Lab Project: 3 Level Elevator & 7-Segment Display

Course: SMRTTECH 3DE3- Digital Electronics

Lab Instructor: Rameez Ashraf

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Submitted by:

Hussein Al-Ansari 400395232

Shehab Ahmed 400359237

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Project Topic Description:

The project centers on designing and implementing a 3-Level Elevator System with a 7-Segment Display, employing either digital logic circuits or FPGA technology. This system is designed to operate seamlessly between three floors, controlled by various input and output components. At the core of the design are push buttons, which allow users to command the elevator to move to a specific floor. Each floor is equipped with LEDs to indicate the elevator's position, while a 7-segment display provides real-time feedback by displaying the current floor number. These features aim to create an intuitive and user-friendly elevator interface.

A key highlight of the project is the opportunity to integrate advanced features that enhance functionality and interface complexity. For example, the 7-segment display could be programmed to flash while the elevator is in transit, signaling activity to the user. Students are encouraged to explore creative solutions and implement additional features that contribute to a better user experience. The challenge lies in making efficient use of limited FPGA ports for input and output while prioritizing which features to develop within the project's constraints.

The elevator system will rely on various hardware components, such as reed switches to detect floor positions and a DC motor controlled via a motor driver circuit to manage vertical movement. The FPGA, programmed using Verilog and Quartus II software, serves as the controller, integrating all components into a cohesive system. This setup provides hands-on experience in hardware-software integration and practical applications of digital logic design.

The expected outcome is a fully operational miniature elevator model that demonstrates smooth interaction among its components. The project will culminate in a detailed documentation report, including wiring diagrams, digital designs, flowcharts, and a summary of operational features. This report will also discuss design decisions, limitations, and achievements.

This project offers a comprehensive learning experience in digital electronics, challenging students to apply engineering principles, creativity, and technical expertise. By completing this project, students will gain valuable insights into system design, FPGA programming, and the practical integration of electronic components in real-world applications.

Resources Used:

Integrated Circuits (ICs):

- **SN754410 Motor Driver IC:** This IC is used to control the DC motor responsible for the elevator's movement. It supports bidirectional control, enabling upward and downward motion of the elevator. The IC is designed for high-current applications, making it suitable for driving inductive loads such as motors.
- **7-Segment Decoder (SN74LS47):** Used a 7-segment display, simplifying the display of floor numbers.
- **Reed Switches:** These are used as position sensors to detect the presence of the elevator at specific floors. They act as triggers for updating the elevator's state.
- **Push Button Switches:** Installed on each floor, these switches allow users to command the elevator to their desired floor.
- **LEDs:** 3 user-controllable LEDs on the board are used for debugging or to indicate system states.

Port/Pin Assignments:

- **DE0-Nano FPGA Board:**
    - **Push Buttons:** Connected to FPGA pins for user inputs. (PIN_A5, PIN_A6)
    - **7-Segment Display Connections:** Outputs from the FPGA (via the decoder IC) drive the 7-segment display. Pins on the FPGA will be mapped to inputs on the decoder IC, which subsequently controls the display.
    - **Reed Switches:** Connected to FGPA pins for user inputs. (PIN_P9, PIN_R10)

Power Supplies:

- **5V and 9V Power Supply:** The 5V power supply drives the ICs and FPGA, while the 9V power supply is used for the DC motor.
- **DE0-Nano Board USB Power:** Provides power to the FPGA during programming and operation.

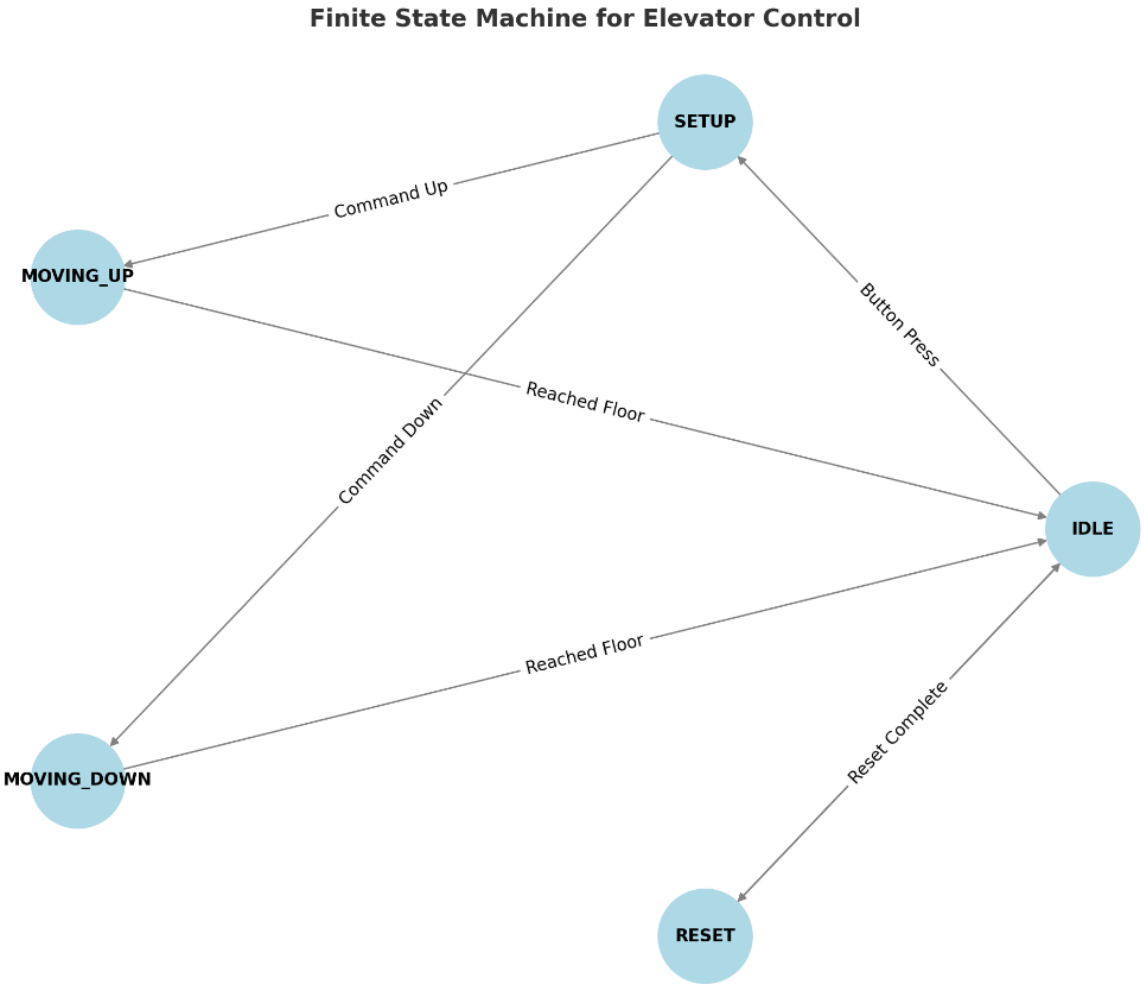
Software and Development Tools:

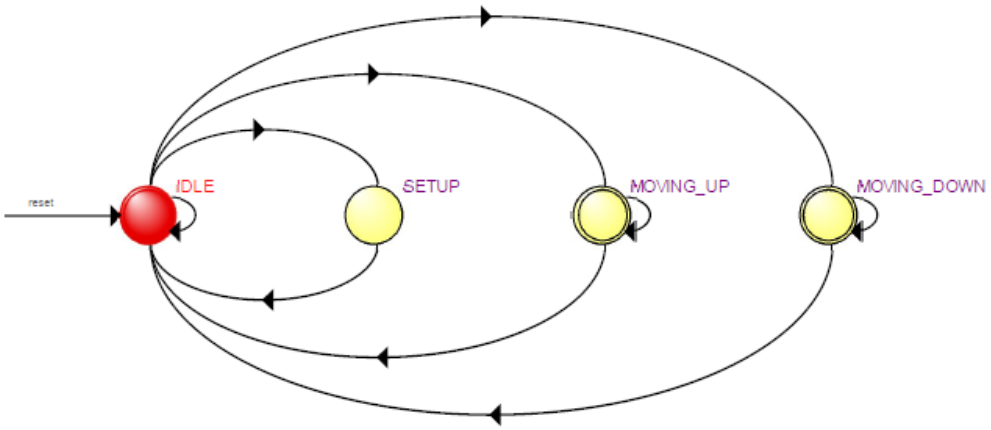
- **Quartus II Software:** Used for writing Verilog code, simulating designs, and programming the FPGA.
- **Multisim:** Utilized for circuit simulation during the design phase.
- **DE0-Nano User Manual:** Serves as a reference for FPGA pin configurations and board usage.

Additional Components:

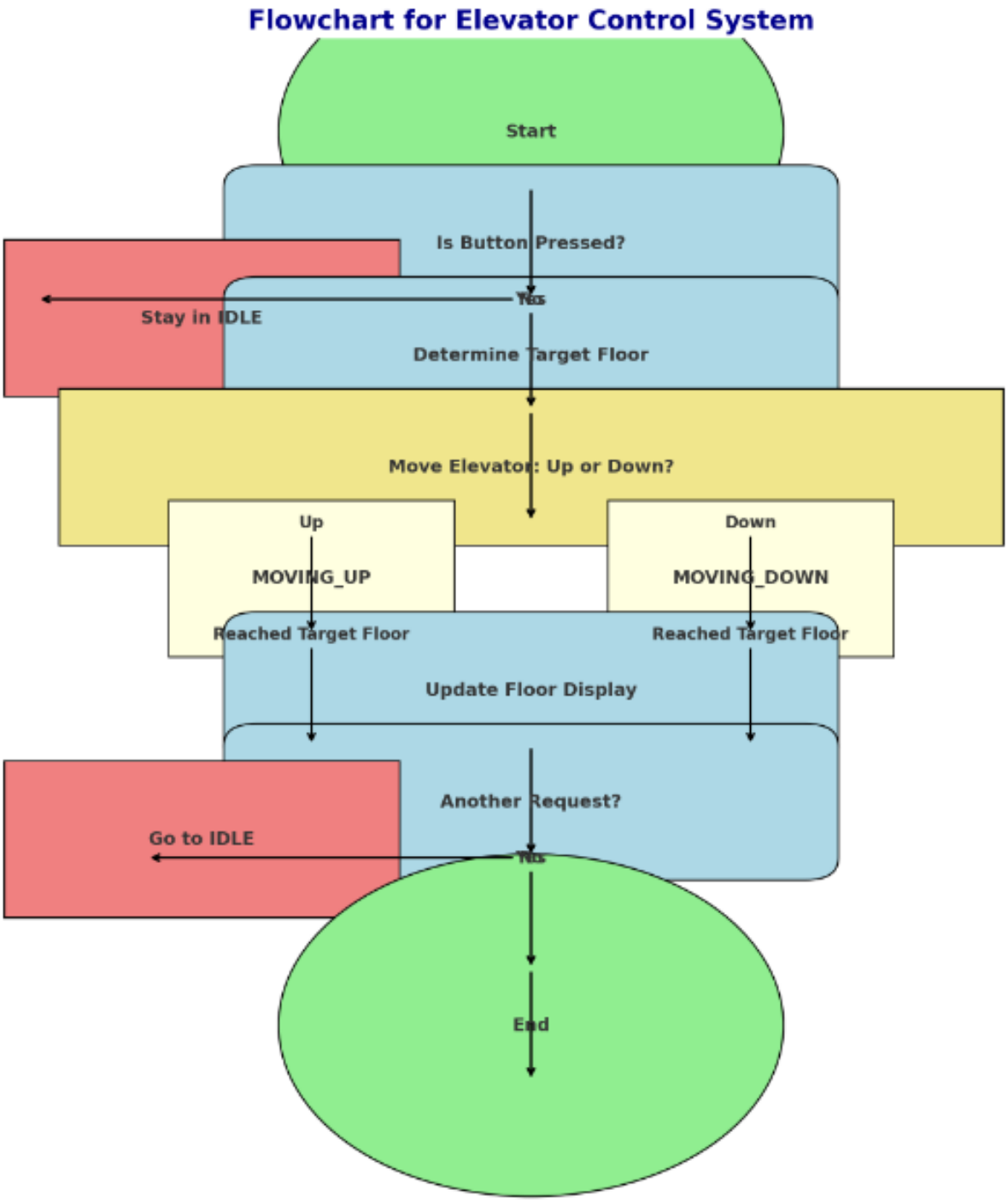
- **Resistors:** Used to limit current for LEDs and other components.
- **Breadboards and Jumper Wires:** Essential for prototyping and connecting components during development.

Digital Design:

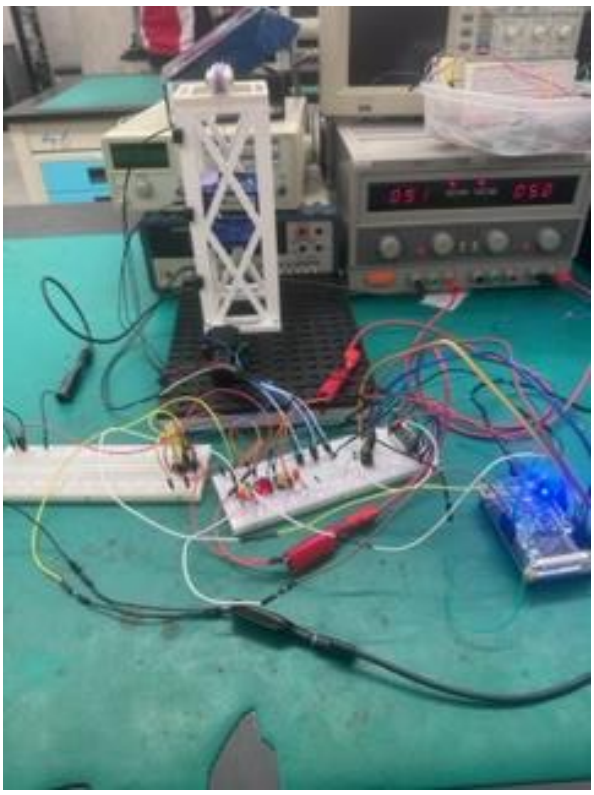


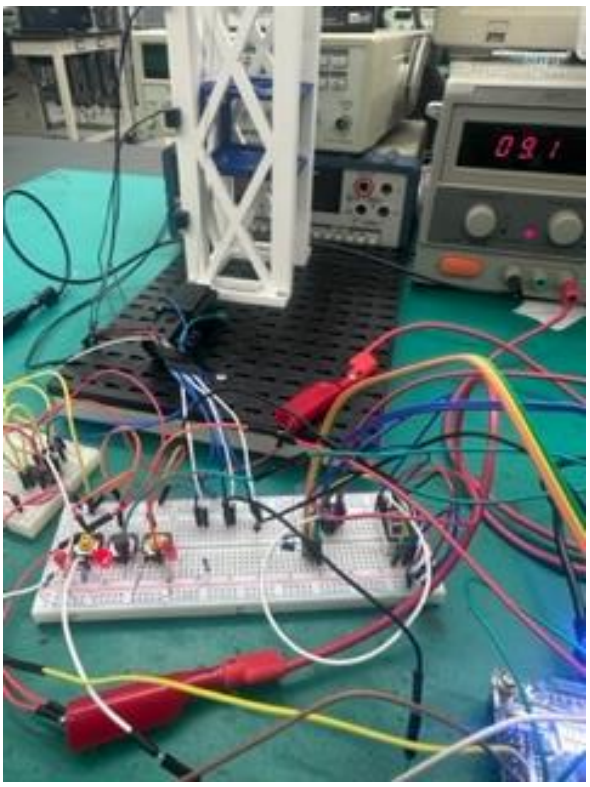


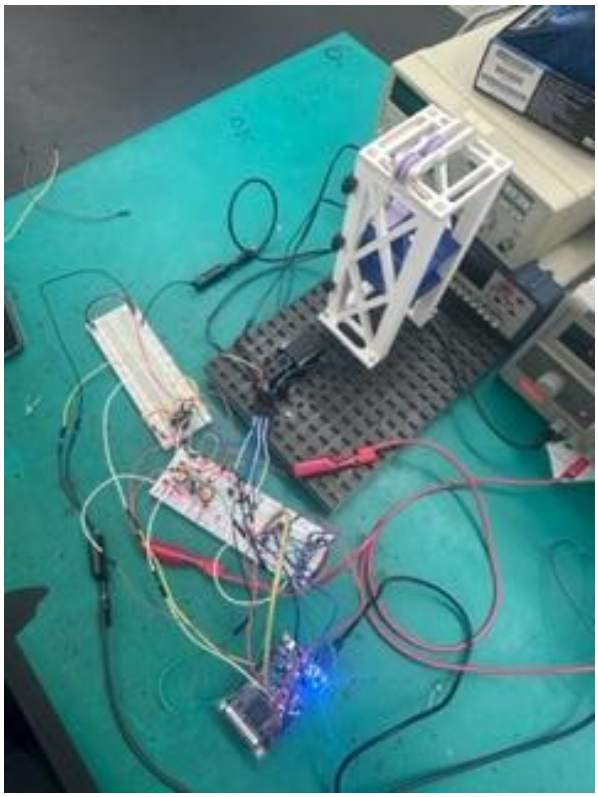
Flow Chart:

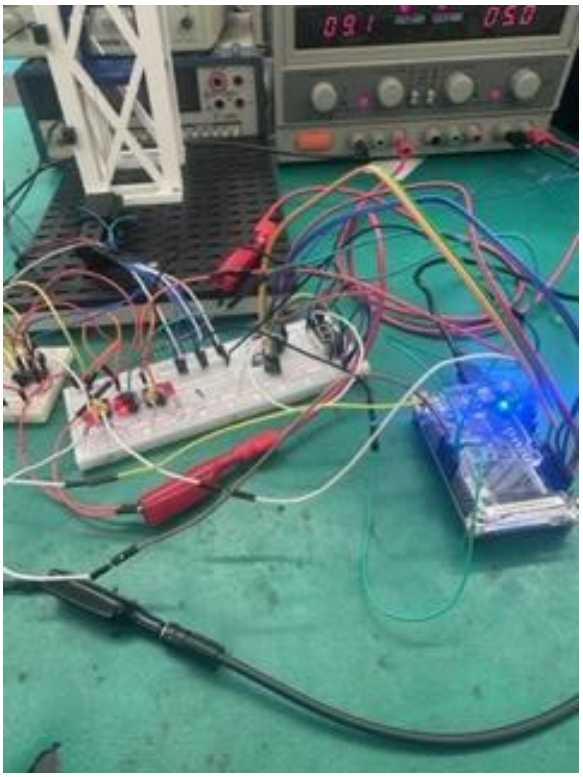

Flowchart for Elevator Control System
Start
Is Button Pressed?
No
Stay in IDLE
Yes
Determine Target Floor
Move Elevator: Up or Down?
Up
MOVING_UP
Down
MOVING_DOWN
Reached Target Floor
Reached Target Floor
Update Floor Display
Another Request?
Yes
Go to IDLE
No
End

Final Setup:

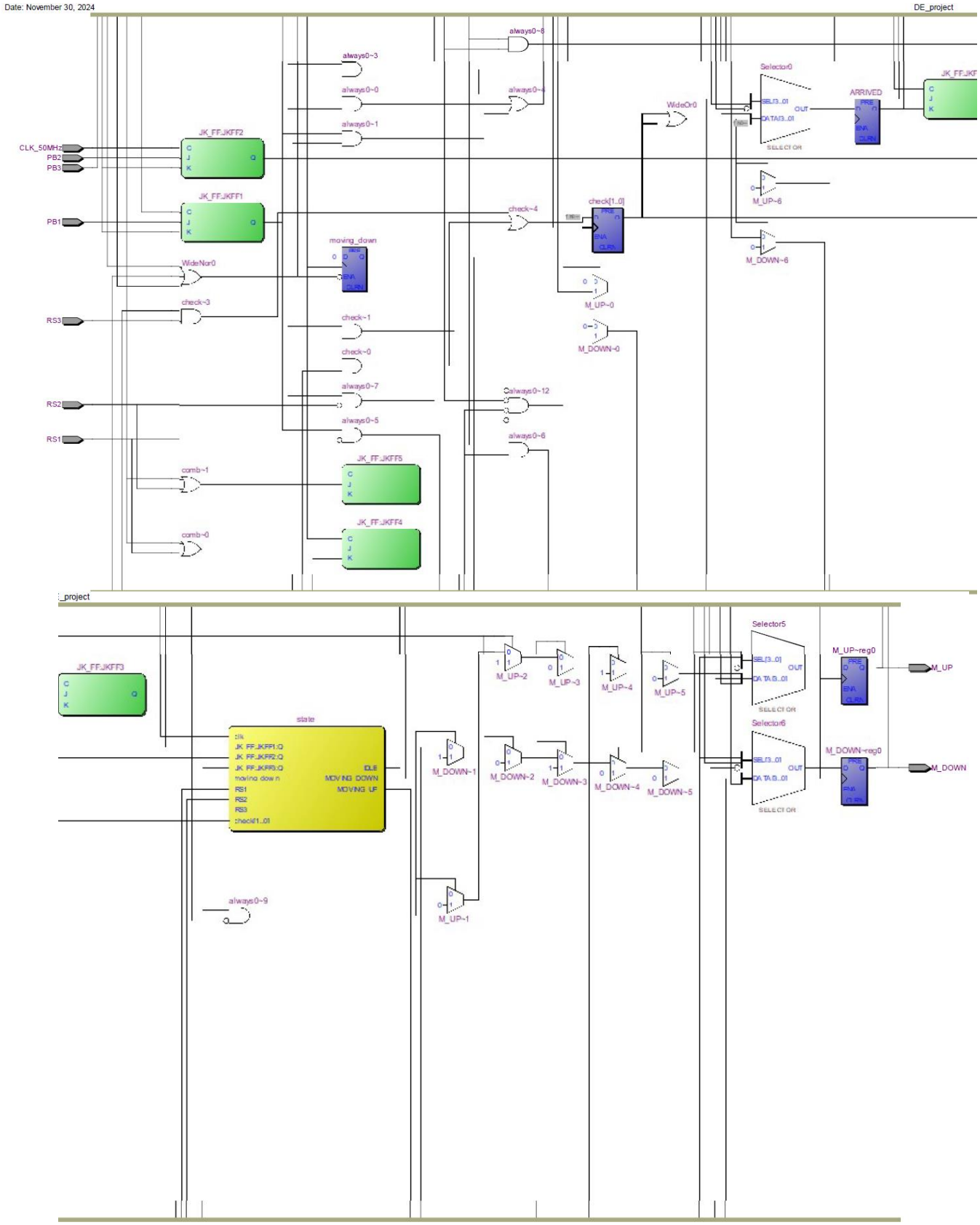








Wiring Diagram:



Discussion:

Project Limitations

1. **Push Button Functionality:**
    - The push buttons did not successfully control the elevator's up-and-down motion as intended. While they could activate LEDs, the signal processing for elevator movement was not properly implemented or debugged.
2. **7-Segment Display:**
    - Although wired correctly, the 7-segment display failed to display the floor number. This could be due to issues in signal mapping, insufficient driving current, or incorrect Verilog implementation for BCD-to-7-segment conversion.
3. **Reed Switches:**
    - The reed switches were not operational, which limited the ability to detect floor positions. This prevented the system from implementing state transitions based on elevator position.
4. **System Debugging:**
    - Insufficient debugging and testing time likely contributed to the inability to fully integrate all components and verify their functionality under real operating conditions.
5. **Limited Feedback:**
    - Without the working 7-segment display and reed switches, the system lacked essential feedback to indicate the elevator's state or current position.

Design Selection

1. **Motor and Motor Driver IC:**
    - The motor driver IC successfully enabled the elevator to move up and down based on control signals from the FPGA. This validated the use of the SN754410 motor driver and the overall motor control design.
2. **Push Buttons for LEDs:**
    - The push buttons successfully turned on the LEDs, demonstrating the basic functionality of the buttons and signal latching via D Flip-Flops in Verilog.
3. **7-Segment Display:**
    - Wiring the display correctly and attempting to interface it with the FPGA were steps in the right direction. However, the absence of displayed numbers indicates a need for further debugging in signal routing or code.
4. **Reed Switches:**
    - Although reed switches were chosen for their simplicity, they were not functional. This highlights the need to either debug the hardware connections or test alternative sensors for position detection.
5. **FPGA as Core Controller:**
    - The DE0-Nano FPGA was a strong design choice, allowing for centralized logic implementation and motor control. Despite incomplete functionality, the FPGA successfully integrated some key system components.

Project Achievements

1. **Motor Control Achieved:**
    - The motor moved up and down as intended, controlled by signals from the FPGA. This demonstrates the successful implementation of motor control logic in Verilog and the proper integration of the motor driver IC.
2. **Push Button and LED Integration:**
    - Push buttons successfully controlled the LEDs, indicating that the basic input-output relationship and D Flip-Flop logic were functional.
3. **Partial Display Setup:**
    - While the 7-segment display did not show numbers, its wiring was completed correctly, and the groundwork for floor indication was established.
4. **Hands-on Debugging Experience:**
    - The challenges faced during the project provided valuable learning opportunities in debugging hardware connections, understanding Verilog implementations, and working with FPGA programming.
5. **Integration of Key Components:**
    - Despite some components not working as expected, the project demonstrated partial integration of motor control, LED indicators, and basic input handling using FPGA technology.

Summary

While the project faced challenges in implementing full functionality, it succeeded in key areas like motor control and basic push button-LED integration. The primary limitations stemmed from incomplete debugging of the push button logic, non-functional reed switches, and 7-segment display issues. Nevertheless, the achievements provide a strong foundation for future iterations, with clear directions for improvement, such as debugging button-floor mapping, testing alternative sensors, and refining display logic. The project demonstrated the potential of FPGA-based control systems and offered significant hands-on learning.

Conclusion:

The project aimed to design and implement a 3-floor elevator control system using FPGA technology, integrating various components such as push buttons, LEDs, a 7-segment display, reed switches, and a motor driver. While the project faced several challenges, it provided valuable insights into digital electronics design, hardware-software integration, and FPGA programming.

Despite some limitations, the project achieved significant milestones. The motor was successfully controlled by the FPGA, moving the elevator up and down as per the programmed logic. Push buttons were able to activate LEDs, demonstrating partial functionality of the input-output control system. Although the 7-segment display did not display numbers as intended, its correct wiring and attempted integration laid the groundwork for future development. The reed switches, however, remained non-functional, highlighting the need for further debugging or alternative design solutions.

The project's challenges underscored the importance of thorough testing, debugging, and timing analysis in FPGA-based systems. The limitations encountered, such as incomplete push button functionality and display issues, offer clear directions for future work. Enhancements could include better signal mapping, debugging reed switch connections, and refining the 7-segment display logic.

Overall, the project provided a robust learning experience, equipping the team with practical skills in Verilog programming, circuit integration, and problem-solving. It demonstrated the potential of FPGA technology for real-world applications and serves as a foundation for more advanced projects in digital electronics and control systems.